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Characterization of Double Gate TFET using Different Dielectric Materials

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Abstract: The Tunnel FET is a new type of transistor. To overcome the large leakage current and Short channel effects (SCEs) of MOSFET, Tunnel FETs are used today. The structure of TFET is approximately similar to MOSFET, however with different switching mechanism. Switching of TFET is done by modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs. TFET has low leakage current and small subthreshold swing (SS) than MOSFET. To improve the ON current and to reduce the leakage current, we are using high-k dielectric materials as gate oxide. In this paper, we propose and validate a novel design for the semiconductor devices with high-k dielectric materials and also the performance is compared for the Double Gate TFET (DG-TFET) by using different gate dielectric materials.

Keywords: SCEs, Leakage current, Subthreshold swing, Tunnel FET, Double Gate Tunnel FET (DG-TFET).

I. INTRODUCTION

In recent years, low power devices with steep switching characteristics has become important. Highly scaled MOSFETs are unsuitable for low power applications due to their switching. When the MOSFET dimension is scaled down to nanometer range (<100 nm), many physical barriers appear, like short channel effects (SCEs) and large leakage current. In order to overcome the short channel effects (SCEs) and reduce the leakage current, small subthreshold swing switches are the interesting candidates to replace or complement the MOSFETs used today[2]. Hence, the Tunnel Field Effect Transistor (TFET) is being designed extensively for low power applications. A TFET has a steep switching characteristics as it works on the phenomena of band-to-band tunneling[1]. The structure of TFET is very similar to MOSFET, but their switching mechanism differs. TFET uses band to band tunneling and MOSFET uses thermionic emission mechanism [8]. In TFET, the ON current is low when compared to MOSFET [8]. But an OFF current is significantly reduced compared to a conventional MOSFET. So the subthreshold swing of the TFET is smaller than MOSFET [2]. This paper explains the structure of Tunnel FET and how it functions (in section II), and discuss the ON current performance of the Double Gate TFET (DG-TFET) by using different gate dielectric materials.

II. DEVICE OPERATION AND STRUCTURE

A. Single Gate TFET (SG-TFET)

In this section, structure of n-type and p-type structures are explained. The structure of a n-type TFET is shown in Figure 1. The device structure of TFET is similar to MOSFET with one exception. In the MOSFET, source and drain are doped with the same type of doping concentrations and the dopant types are opposite to that of substrate, while in a TFET, source and drain are of opposite doping types and the drain region has a doping concentration same as that of substrate with higher concentration. In n-type TFET, drain region has n-type doping type as same as that of substrate with high concentration [6]. Similarly in p-type TFET, drain region has p-type doping type as same as that of substrate with high concentration as shown in figure 2.

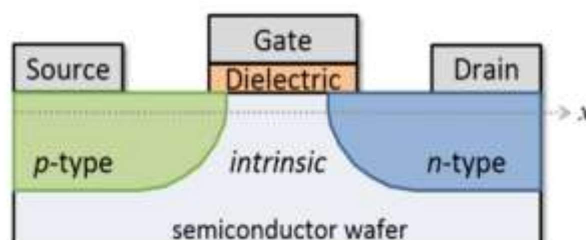

Fig. 1. Structure of n-type TFET

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TFET includes the characteristics of many devices: 1) In OFF state, it works like reversed P-I-N diode, 2) In ON state, it operates as Esaki tunnel diode, 3) When gate voltage is applied, it works as the MOS diode to form the inversion or accumulation layer.

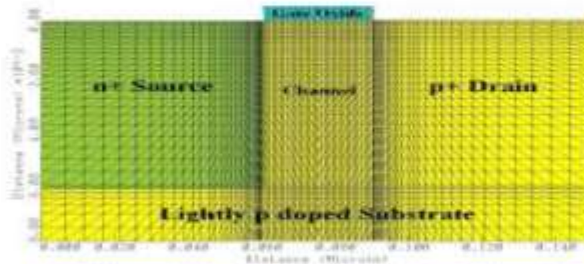

Fig. 2. Basic structure of P-type TFET (PTFET)

The doping concentration of the source and dra in is 10^{20} cm^{-3} and for substrate and channel, the doping concentration is 10^{15} cm^{-3} so that the channel behavior is intrinsic. Channel doping concentration (NCH) is varied later to study the effect of channel concentration on device performance.

B. Working principle of TFET

In thermal equilibrium of a TFET, there is no external bias (VG = VS = VD = 0). There are two depletion regions formed – one at the source–channel junction and the other at the channel–drain junction [7]. When TFET is in equilibrium, the built-in potentials of the P-I and I-N junctions results in a staircase like band profile as shown in figure 3. When TFET is in OFF-state, the P-I-N diode is reverse biased. This leads to a thick tunneling barrier between valence band and conduction band in the region of operation. The thick tunneling barrier reduces the tunneling probability. This leads to a very small off state current. When TFET is in ON-state, the tunneling barrier width reduces. So the electrons are moving from valance band of the source to the conduction band of the channel and then reach to the conduction band of drain. This process is called as band to band (BTBT) tunneling is the main reason for the source carrier injection. Because of the presence of the BTBT barrier, ON currents and OFF currents of TFETs are always lower than conventional MOSFETs [7].

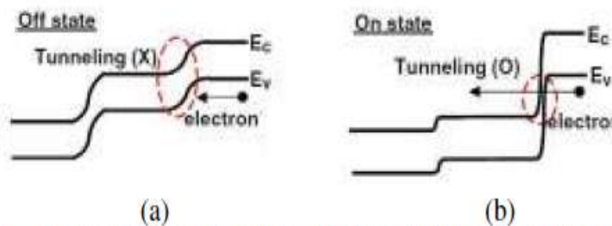

Fig. 3. Schematic Band diagram of a TFET in (a) Off state and (b) On state to illustrate the tunneling phenomenon

When VGS > VTH, The n-type TFET is switched on and when VGS < VTH the p-type TFET is switched on. In OFF state, the P-I-N diode is always reverse biased thus results in an ultra-low leakage current. For n-type TFET, substrate is lightly n-doped. The increasing gate voltage results in an accumulated n region. So the electrons tunnel the tunneling junction of Gate OXide (GOX)/channel/p+ doped region [7]. In a n-type TFET, when a gate bias is applied, electrons tunnel from the p+ doped region into the channel and then flow into the n+ doped region. In n-type TFET, the p+ doped region is named as source (source of electrons) and the n+ doped region is name as drain (drain of electrons). When VGS > VTH, the n-type TFET is switched on. When negative gate voltage is applied to the gate, an inversion layer will be formed and tunneling junction will move to the cross point of GOX/channel/n+ doped region. For p-type TFET the substrate is lightly p-type doped. When negative voltage is applied to the gate, an accumulated hole channel is formed. So the electrons tunnel through the cross point of GOX/channel/n+ doped region [7]. In this, the electrons tunnel from the p+ channel region to the n+ doped region and the generated holes in the channel flow to the p+ doped region. Therefore, in the case of n-type TFET, the p+ doped region is named as drain (drain of holes) and the n+ doped region is called as source.

C. Transfer characteristics of TFET

The Figure 4 shows the transfer characteristics of TFET. As the gate bias increases, the current rapidly increases due to reduction of the tunneling width and an increase in the number of initial states in the source from where tunneling can

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occur. At a higher gate bias, the rate of increase of current reduces [5]. As the gate bias approaches the drain potential, the rate of increase of current further decreases due to pinning. A similar behaviour is observed in the negative bias region. This behaviour of the TFET is referred to as ambipolar operation.

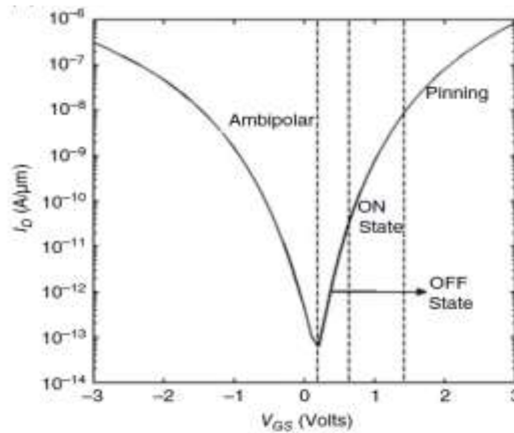

Fig. 4. Transfer characteristics of TFET

D. Double Gate TFET (DG-TFET)

The Figure 5 shows the structure of a double gate TFET. It consists of two gates, one at the top (called the front gate) and the other at the bottom (called the back gate) [4]. This configuration improves the electrostatic control of the gate on the channel since now the field lines from the gate terminate at the back gate rather than terminating in the channel. The ON-state current is also increased when compared to the single gate TFET (SG-TFET), since there are two channels in which higher amount of current can flow in the device.

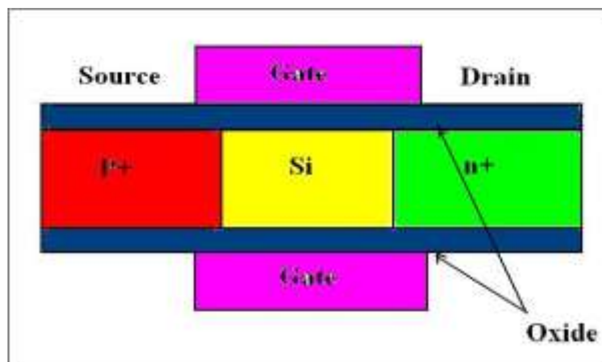

Fig. 5. Schematic of a p-channel double gate (DG) TFET

In Double gate Tunnel-FET, the current is doubled because of applying two gate voltages. Hence, the ON-current is larger than single gate TFET OFF-current is lower. In TFET for different values of V_{ds} voltage and I_{off} is decreasing. Comparing this with MOSFET, this is good achievement in energy saving in low power devices.

E. High-k dielectric

The term **high-k dielectric** material is nothing but a material with a high dielectric constant k (as compared to silicon dioxide).

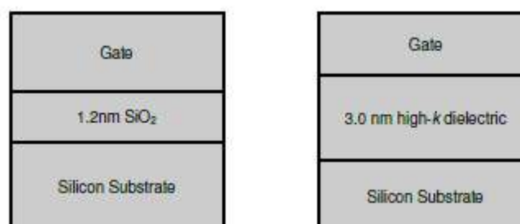

Fig. 6. Replacing SiO_2 with high-k dielectric material

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High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or any other dielectric material of a device to improve the ON current of the device. Silicon dioxide (SiO_2) has been used as a gate oxide material for decades. As transistors are in reduced size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. But, the leakage current is increased due to increased gate capacitance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leads to high power consumption and reduced device reliability. In Figure 6, replacing the silicon dioxide gate dielectric with a high-k material allows increased gate capacitance without producing the leakage currents is shown. An even higher ON -current and decreased subthreshold swing can be achieved by the careful choice of a gate dielectric materials. As shown in Figure 7, current increases when the gate dielectric constant increases. Here, Si_3N_4 and two high-k dielectrics, HfO_2 and ZrO_2, are compared with SiO_2. The high-k materials have dielectric constants of 21 and 29, respectively.

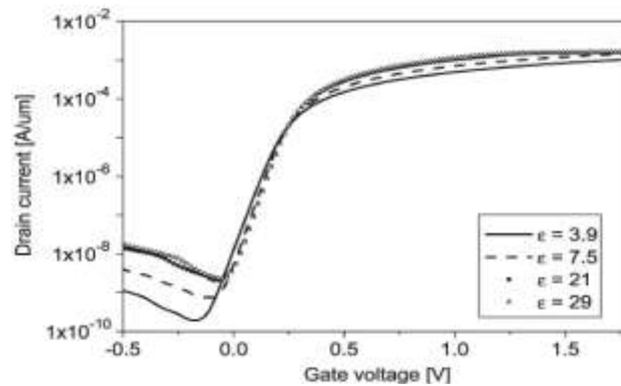
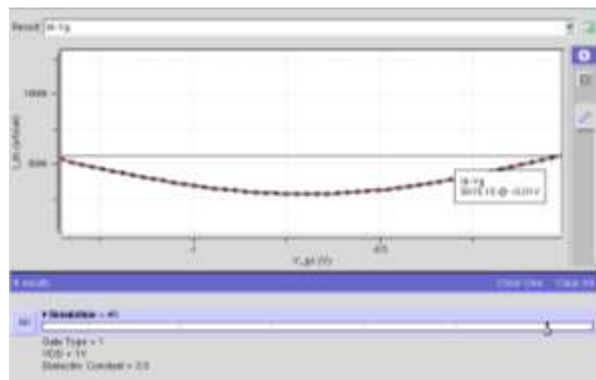


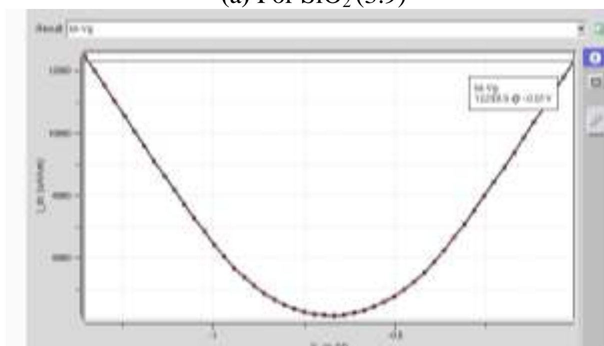
Fig. 7. DG-Tunnel-FET characteristics for various gate dielectrics

III. RESULTS AND DISCUSSION

The reduced gate oxide thickness provided by these dielectrics offers a solution to the low ON current problem experienced by some existing Tunnel FETs. The OFF-current is less than 1 fA. All simulations were done in NanoHub software, which uses band to band tunneling model.



(a) For SiO_2 (3.9)



(b) For HfO_2 (25)

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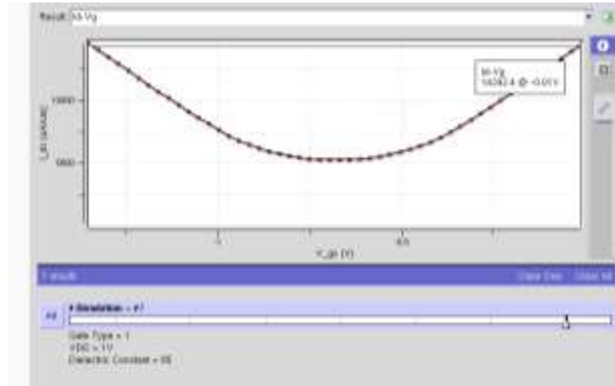

(c) For TiO_2 (85)

Fig.8. I-V characteristics of TFET using High-k Dielectrics

The Table 1 shows the comparison of ON current for different gate materials with different dielectric constants.

TABLE I COMPARISON OF ON CURRENT OF DIFFERENT DIELECTRIC MATERIALS

Material	Dielectric Constant	ON current, I_{ON}
SiO_2	3.9	5615.18 μA/μm
HfO_2	25	12299.9 μA/μm
TiO_2	85	14392.4 μA/μm

IV. CONCLUSION

To reduce the short channel effects (SCEs) and to reduce the leakage current so in replacement to MOSFET, Tunnel FET (TFET) is used. Further to reduce the level of OFF current in TFET and to improve the performance of the device, the Double Gate TFET with high-k dielectric materials are designed and the ON current of the DG-TFET with different high-k materials are compared. In this, the ON current of DG-TFET with TiO_2=85 is higher when compared to the materials SiO_2 and HfO_2.

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